Abstract of the Disclosure

The preferred embodiments described herein provide a memory device and method for storing bits in non-adjacent storage locations in a memory array. In one preferred embodiment, a memory device is provided comprising a register and a memory array. A plurality of bits provided to the memory device are stored in the register in a first direction, read from the register in a second direction, and then stored in the memory array. Bits that are adjacent to one another when provided to the memory device are stored in non-adjacent storage locations in the memory array. When the plurality of bits takes the form of an ECC word, the storage of bits in non-adjacent storage locations in the memory array reduces the likelihood of an uncorrectable multi-bit error. In another preferred embodiment, a memory device is provided comprising a memory array and a register comprising a first set of wordlines and bitlines and a second set of wordlines and bitlines arranged orthogonal to the first set. In yet another preferred embodiment, memory decoders or a host device is used to store bits in non-adjacent storage locations in a memory array of a memory device. Other preferred embodiments are provided, and each of the preferred embodiments described herein can be used alone or in combination with one another.